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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,753	01/20/2004	Karl Edwards	LT-106 Div. 2	2868

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,753	EDWARDS, KARL	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20012004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because transistor (610) in figure 6 is supposed to be an PNP transistor (see spec. page 14). Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claims 1 and 2, the recitation "1) at the first state, a current is conducted by the SET circuit wherein the SET circuit is maintained such that a first switching threshold is obtainable by using the first trigger signal 2) at the second state, the current is conducted by the RESET circuit wherein the RESET circuit is maintained such that a second switching threshold is obtainable by using the second trigger signal" is confusing because it is nor clear

how the 'first switching threshold" and the "second switching threshold" can be obtained and how the SET and the RESET circuits are maintained. The recitation " 3) a combination of 1 and 2" is indefinite because it is not clear how the SET state (first state) can combined with the RESET state (second state) to create a third state that is the combination of the first state and the second state. Clear explanation is required. The Applicant is requested to show what drawing the circuits of claims 1 and 2 read on and to show in the drawing the "SET circuit", "RESET circuit", the " an output" of the latch circuit and where in the circuit the first and second trigger signals are applied to.

Regarding claim 4, the recitations "a first latch transistor", "a second latch transistor", "a SET transistor" and "a RESET transistor" are indefinite because they cannot be identified in the drawing. The Applicant is requested to point out these elements in the drawing and in the specification. The recitation "1) at the first state....3) a combination of 1) and 2)" on lines 13-22 is indefinite because of the same reason pointed out in the 112, 2nd rejection of claims 1 and 2.

Claim 5 is indefinite because many elements cannot be identified in the circuit for instance the "output of an oscillator", "a first latch transistor", a second latch transistor", "a SET transistor", "a RESET transistor" and " a first current". The recitation "at the first state, conducting a first current in the first latch transistor **and** the SET transistor such that the SET transistor is biased at a point close to a first threshold; at the second state, conducting the first current in the second latch transistor and the RESET transistor such that the RESET transistor is biased at a point close to a second threshold" is indefinite because it is not clear how at the first state a **first current** can be conducted by two transistors (first latch transistor and SET transistor) and at the second state how a **first current** can be conducted by two other transistors (second latch transistor and RESET transistor). The recitation "varying the output from the first state to the second state by providing a trigger current to raise the base of the SET transistor over a **first threshold**; and varying the output from the second state to the first state by providing the trigger current to raise the base of the RESET transistor over a **second threshold**" is indefinite because it is confusing. It is not clear how a **trigger current** applied to the **base** of a transistor can raise the base of the transistor to **a threshold** (first or second). The Applicant is request to explain what the "a first threshold" and the "a second threshold" are

meant by and to explain how a trigger current applied to the base of a transistor can raise its threshold. The Applicant is requested to point out what drawing the circuit of claim 5 reads on.

Claim 6 is indefinite because of the technical deficiencies of claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Nolan et al. (US Pat. 6,020,792).

Regarding claims 1, 2, 3 and 4, figure 3 of Nolan shows a latch circuit having an output (166), the output having a first state and a second state, the output being controllable by a first trigger signal (162) and second trigger signal (164), the latch circuit comprising:

a SET circuit, not shown, having an input connected to the (S) input;

a RESET circuit not shown, having an input connected to the (R) input.

The SET/RESET flip-flop circuit has the following basic function (see attached US Pat. 5,541,544): when a first trigger signal applied to the (S) input reaches a first threshold, a current is conducted by the SET circuit and the SET output (Q) is high. When a second trigger signal applied to the (R) input reaches a second threshold, a current is conducted by the RESET circuit and the RESET output (QN) is high. In the third case when the SET and RESET input are both high or low, the flip-flop is in the invalid state or remember state. Figure 3 of Nolan shows that the latch circuit forms a switching portion of an oscillator circuit. Figure 3 is a circuit of a temperature-compensated oscillator circuit (Abstract and col.3, lines 55-66). The level-shifting circuit is circuit 150.

Regarding claims 5 and 6, figure 3 of Nolan shows a method oscillating the output an oscillator, the output having a first state and a second state, the oscillator including a latch (160), the latch including a first latch transistor a second latch transistor, a SET transistor and a RESET transistor (well known, not shown including in circuit 160), the method comprising:

at the first state, conducting a first current in the first latch transistor and the SET transistor such that the SET transistor is biased at a point close first threshold by the SET input signal);

at the second state, conducting the first current in the second latch transistor and the RESET transistor such that the RESET transistor is biased at a point close to a second threshold (by the RESET input signal);

varying the output from the first state to the second state by providing a trigger current raise the base of the SET transistor over a first threshold; and varying the output from the second state to the first state by providing the trigger current to raise the base of the RESET transistor over second threshold. Note that the above method of functioning a SET/RESET flip-flop is basically well known (see reference 5,541,544). By applying a signal to a SET/RESET in put of the SET-RESET flip-flop, the outputs of the flip-flop change states when the input signals of the flip-flop circuit reach the thresholds of the SET/RESET transistors. Figure 3 shows a temperature-compensating oscillator.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

08/11/04

TUAN T. LAM
PRIMARY EXAMINER